

REMARKS

In the present Application, Claims 1-8 and 12-16 are pending. Claims 1-8 and 12-16 are rejected. By this response, Claims 1-8 and 12-16 continue without amendment. In view of the following discussion, the Applicant submits that none of the claims now pending in the application are indefinite under the provisions of 35 U.S.C. §112 or anticipated under the provisions of 35 U.S.C. §102. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. Objections

The Examiner objected to the drawings as failing to show every feature of the invention specified in the claims. In particular, the Examiner stated that the drawings do not show the interposing structure "inside the integrated circuit package" between the IC die and the inside surface of the IC package, as recited in Applicant's claims 1 and 12. (Office Action, p. 2).

The Applicant refers the Examiner to FIG. 10, which shows a die 1011 inside a package 1012. The package 1012 completely surrounds the die 1011. An embodiment of an interposing structure, a caposer 1018, is shown between the die 1011 and the package 1012. The package 1012 also surrounds the caposer 1018. Further, the package 1012 includes two surfaces, e.g., an inside surface 1017 having lands 1014 and an outside surface opposite the inside surface 1017 that includes solder balls 1023. Thus, Applicant's FIG. 10 clearly supports the interposing structure being inside the integrated circuit package between the die and the inside surface of the package.

In view of the foregoing, the Applicant contends that the drawings show all of the features of the claimed invention. The Applicant respectfully requests that the present objection be withdrawn.

II. Rejection of Claims under 35 U.S.C. §112

Claims 1-8 and 12-16 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner stated that in claims 1 and 12, it is unclear what is meant by an interposing structure disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the package. The Examiner requested that the Applicant explain the claimed structure as it relates to the drawings and specification. (Office Action, p. 3).

The Applicant refers the Examiner to FIG. 10, which shows a die 1011 inside a package 1012. The package 1012 completely surrounds the die 1011, and hence the die 1011 is inside the package 1012. Further Applicant's specification states "[a]n integrated circuit die 1011 is mounted within an integrated circuit package 1012." (Applicant's specification, para. 0089). An embodiment of an interposing structure, a caposer 1018, is shown between the die 1011 and the package 1012. The package 1012 also surrounds the caposer 1018. Further, the package 1012 includes two surfaces, e.g., an inside surface 1017 having lands 1014 and an outside surface opposite the inside surface 1017 that includes solder balls 1023. Applicant's specification states "[a] caposer 1018 is disposed between inside upper surface 1017 of ceramic package 1012 and surface 1016 of die 1011." (Applicant's specification, para. 0090). Thus, Applicant's FIG. 10 and paragraphs 0089-0090 of Applicant's specification clearly describe an interposing structure being inside the integrated circuit package between the die and the inside surface of the package.

Furthermore, Applicants contend that the feature of the interposing structure being disposed inside an IC package is clear on its face within the claims as understood by one skilled in the art. That is, one skilled in the art would understand that a die and interposing structure can be positioned within or inside an surrounding structure, such as an integrated circuit package.

In view of the foregoing, the Applicant contends that the cited language in claims 1 and 12 is clear and definite to one skilled in the art when interpreted in light of

Applicant's specification. The Applicant respectfully requests that the present rejection be withdrawn.

III. Rejection of Claims under 35 U.S.C. §102

Claims 1-8 and 12-16 are rejected under 35 U.S.C. §102(e) as being anticipated by Edwards et al. (U.S. Patent No. 6,541,365) ("Edwards"). The rejection is respectfully traversed.

The Examiner cited FIGs. 1-4 in Edwards as showing: an IC die 20 having an array of micro-bumps 33; an IC package 10 having an array of landing pads 12 disposed on an inside surface of the IC package and an array of solder balls disposed on an outside surface of the IC package; and an interposing structure 25 disposed inside the IC package between the IC die and the inside surface of the IC package. (Office Action, p. 4). Applicant respectfully disagrees.

First, Edwards describes the element 33 as a "reduced contact area", not a micro-bump. (Edwards, col. 5, lines 13-15). The IC die 20 in Edwards does include solder balls 16. However, the Examiner is citing the solder balls 16 as Applicant's array of solder balls. Assuming the Examiner's interpretation, there is no element or structure in Edwards that teaches or suggests an array of micro-bumps disposed on a surface of the IC die.

Second, the solder balls 16 in Edwards are not disposed on an outside surface of the package 10. That is, the package 10 includes the landing pads 12 on one surface, and the solder balls 16 are coupled to the landing pads 12 on the same surface. The solder balls 16 in Edwards are not disposed on any surface of the IC package 10. Even if the solder balls 16 of Edwards can be considered to be disposed on a surface of the IC package 10, the surface is the same as that on which the landing pads 12 are disposed. In Applicant's claims, the array of landing pads is on an inside surface of the package, and the array of solder balls is on an outside surface of the package.

Further, Applicant's claims 1 and 12 recite that the interposing structure electrically couples a first micro-bump in a first position of the array of micro-bumps to a first landing pad located opposite the first position and to a second landing pad in the array of landing pads. As noted above, Edwards does not include any elements that can be considered micro-bumps. To the extent the solder balls 16 in Edwards are considered micro-bumps, each of the solder balls 16 is only coupled to a single landing pad 12. There is no teaching or suggestion in Edwards that any of the solder balls 16 is coupled to more than one landing pad, as recited in Applicant's claims.

Applicants note that, in Edwards, the landing pads 18 and the landing pads 12 are in two different arrays. That is, in Edwards, the landing pads 18 are disposed on the die 20, and the landing pads 12 are disposed on the substrate 10. In Applicant's claims 1 and 12, the first micro-bump is electrically coupled to a first landing pad and a second landing pad in the same array of landing pads, which is disposed on an inside surface of the IC package. Edwards is devoid of any teaching or suggestion of such feature.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."  
Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Edwards fails to teach or suggest the various features discussed above. As such, Edwards does not teach each and every element of Applicant's claims 1 and 12 as arranged therein. Accordingly, Chung does not anticipate Applicant's invention recited in claims 1 and 12.

Claims 2-8 and 14-16 depend, either directly or indirectly, from claims 1 and 12 and recite additional features therefor. Since Edwards does not anticipate Applicant's invention as recited in claims 1 and 12, dependent claims 2-8 and 14-16 are also not anticipated and are allowable.

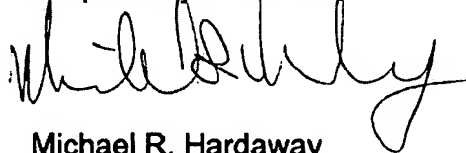
Therefore, the Applicant contends that claims 1-8 and 12-16 are not anticipated by Edwards and, as such, fully satisfy the requirements of 35 U.S.C. §102. The Applicant respectfully requests that the present rejection be withdrawn.

IV. CONCLUSION

Thus, Applicant submits that none of the claims presently in the application are indefinite under the provisions of 35 U.S.C. §112 or anticipated under the provisions of 35 U.S.C. §102. Consequently, Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Applicant's Attorney at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



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*I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on November 25, 2008.*

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